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shield materials includes a strip.

8. The method of claim 5 where said at least one of said patterned magnetic shield materials includes crosses.

9. The method of claim 5 where said at least one of said patterned magnetic shield materials includes bars.

10. The method of claim 5 where said at least one of said patterned magnetic shield materials includes loops.

11. The method of claim 5 where at least some of said patterned magnetic shield materials are formed in a bit plane of said memory array.

12. The method of claim 5 where at least some of said patterned magnetic shield materials are formed in a different plane than a bit plane of said memory array.

13. The method of claim 1 where:

- (1) said magnetic shielding includes a plurality of magnetic particles; and
- (2) said (b) includes:
 - (A) forming an insulating oxide between some of said magnetic memory cells; and
 - (B) embedding said plurality of magnetic particles in said insulating oxide.

14. A method for manufacturing a magnetic shield in a magnetic memory array, said magnetic memory array comprising a plurality of magnetic memory cells on a substrate, said method comprising:

- (a) forming at least a portion of a magnetic shield layer:
 - (1) in a different plane than a bit plane of said memory array; and
 - (2) adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to another of said magnetic

memory cells; and

- (b) forming an insulator separating at least a portion of said magnetic shield layer from said at least one magnetic memory cell.

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15. A method for manufacturing a magnetic shield in a magnetic memory array, said memory array comprising a plurality of magnetic memory cells on a substrate, said method comprising:

- (a) forming patterned magnetic shield materials adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to another of said magnetic memory cells; and
- (b) forming an insulator separating at least a portion of said patterned magnetic shield materials from said at least one magnetic memory cell.

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16. A method for manufacturing a magnetic shield in a magnetic memory array, said memory array comprising a plurality of magnetic memory cells on a substrate, said method comprising:

- (a) forming a plurality of magnetic particles adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to another of said magnetic memory cells; and
- (b) forming an insulator separating at least a portion of said plurality of magnetic shield particles from said at least one magnetic memory cell:
 - (1) said insulator including an insulating oxide between said magnetic memory cells; and
 - (2) said magnetic particles being embedded within said insulating oxide.

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17. A magnetic shield for reducing magnetic interference between at least two magnetic memory cells in a magnetic memory array, said memory array comprising a plurality of magnetic memory cells, each of said magnetic memory cells including a data layer and a reference layer, wherein a value stored in said data layer is determinable by measuring a relative orientation of the magnetic moments of said data layer and said reference layer, at least one of said magnetic memory cells during

operation emanating fringe magnetic fields potentially influencing a nearby magnetic memory cell, said magnetic shield being made by a process comprising:

- (a) forming a magnetic shielding adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to another of said magnetic memory cells; and
- (b) forming an insulator separating at least a portion of said magnetic shielding from said at least one magnetic memory cell.

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18. A magnetic shield for reducing magnetic interference between at least two magnetic memory cells in a magnetic memory array, said magnetic shield being made by a process comprising:

- (a) forming a magnetic shield layer:
 - (1) in a different plane than a bit plane of said memory array; and
 - (2) being disposed adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to another of said magnetic memory cells; and
- (b) forming an insulator disposed as to separate at least a portion of said magnetic shield layer from said at least one magnetic memory cell.

19. A magnetic shield for reducing magnetic interference between at least two magnetic memory cells in a magnetic memory array, said magnetic shield being made by a process comprising:

- (a) forming patterned magnetic shield materials adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to another of said magnetic memory cells; and
- (b) forming an insulator separating at least a portion of said patterned magnetic shield materials from said at least one magnetic memory cell.

20. A magnetic shield for reducing magnetic interference between at least two magnetic memory cells in a magnetic memory array, the magnetic shield being made by a method comprising:

- (a) forming a plurality of magnetic particles adjacent to at least one of said magnetic memory cells to reduce magnetic interference with respect to

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another of said magnetic memory cells; and

- (b) forming an insulator disposed as to separate at least a portion of said plurality of magnetic shield particles from said at least one magnetic memory cell:

- (1) said insulator including an insulating oxide between said magnetic memory cells; and
- (2) said magnetic particles being embedded within said insulating oxide.